REMARKS/ARGUMENTS

1. Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

2. Rejection of claims 11, 19, and 33-36 under 35 U.S.C. 102(e):

Claims 11, 19, and 33-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Sutardja et al. (US 6,903,448).

Response:

Claims 11, 19, 33, and 35 have been cancelled, and are no longer in need of consideration. Claim 35 has been amended to distinguish from Sutardja. Claim 35 now recites that "each bonding pad is connected to one of the package substrate and the corresponding first lead frame with the other of the package substrate and the corresponding lead frame remaining unconnected, thereby providing two types of bonding options for each bonding pad". Claim 35 also states that "the connection of the bonding pad is determined according to the functionality of the chip".

This amendment is fully supported in the end of paragraph [0021], which states the following:

> Because one chip usually has different functions or configurations, some pins of the chip must be given their voltage, Enable or Disable, before the chip is packaged. Enable is usually represented by a high voltage of logic "1" (voltage of the power supply). When one pin of a chip is connected to a power supply, some function of the chip is enabled. In contrast, Disable is usually represented by a low voltage of logic "0" (voltage of the ground). When one pin of a chip is connected to ground, some function of the chip is disabled. Enable and Disable make it possible that one chip with many functions can be set to one of the functions according to different applications. Also, Enable and Disable

representing logic "1" and logic "0" can be used for testing chips.

In contrast, Sutardja does not teach that bonding pads are connected to the die paddle 1 or the leads 72 according to the functionality of the chip, and only teaches that the die paddle 1 or the leads 72 are used for providing voltage values. For these reasons, the currently amended claim 35 is patentable over Sutardja.

Regarding claim 36, Sutardja does not teach the claimed method. Specifically, Sutardja does not teach providing two identical package substrates for two identical chips, with each chip comprising a plurality of bonding option units having a corresponding bonding pad. Moreover, Sutardja does not teach for one of the chips connecting at least one predetermined bonding pad of the said bonding pads to the corresponding package substrate, while for the other chip connecting at least one bonding pad equivalent to the said at least one predetermined bonding pad to the corresponding first lead frame such that identical chips are packaged to different ICs. Sutardja only teaches a single chip 2, and does not teach an identical chip having different bonding pad connections as claimed. Therefore, claim 36 is patentable over Sutardja.

In view of the above, reconsideration of claims 35 and 36 is respectfully requested.

3. Introduction to new claims 37-42:

New independent claim 37 recites a method of packaging a chip, which involves connecting a package substrate to a high or low voltage, and providing a plurality of first lead frames having the opposite voltage level of the package substrate. Then connections of the bonding pads of the bonding option units are determined according to the functionality of the chip.

In contrast, Sutardja does not teach that bonding pads are connected to the die paddle 1 or the leads 72 according to the functionality of the chip, and only teaches that the die paddle 1 or the leads 72 are used for providing voltage values. For these

reasons, new claim 37 is patentable over Sutardja.

Dependent claims 38-42 specify that the bonding pads are connected to the package substrate, the first lead frames, or second lead frames for enabling or disabling the functionality of the chip in different applications. These claims are supported in paragraph [0021], and no new matter is added. Since Sutardja does not teach that the bonding pads are connected to the package substrate, the first lead frames, or second lead frames for enabling or disabling the functionality of the chip in different applications, claims 38-42 are patentable over Sutardja as well.

Consideration of new claims 37-42 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 05/08/2007

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)